REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed March 2, 2006. Upon entry of the amendments in this response, claims 1, 3 – 12, 14 – 19, 22, 25 and 26 are pending. In particular, Applicants have amended claims 1, 3 – 6, 10, 14 – 17, 19 and 22, have added claims 25 and 26, and have canceled claims 13, 20, 21, 23 and 24 without prejudice, waiver, or disclaimer. Applicants have canceled claims 13, 20, 21, 23 and 24 merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicants reserve the right to pursue the subject matter of this canceled claim in a continuing application, if Applicants so choose, and do not intend to dedicate the canceled subject matter to the public. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections Under 35 U.S.C. §101

The Office Action indicates that claims 1 and 3 - 24 stand rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. As set forth above, Applicants have canceled claims 13, 20, 21, 23 and 24, and respectfully assert that the rejection as to these claims has been rendered moot. With respect to the remaining claims, Applicants respectfully traverse.

In this regard, Applicants have amended claims 1, 3 – 6, 10, 14 – 17, 19 and 22 and respectfully assert that the rejections have been accommodated. However, to the extent that the rejections are otherwise improper for lacking in legal basis, Applicants respectfully assert that claims 1, 3 – 9, 19, 25 and 26 are directed to methods. As defined by Congress, 35 U.S.C. §101 recites that, among others, a "process" is statutory subject matter. In that a method is a process, Applicant submits that claims 1, 3 – 9, 19, 25 and 26 are directed to statutory subject matter. Additionally, with respect to claims 10 – 12 and 14 – 18, these

claims are directed to a system that includes structural components, and claim 22 is directed to an integrated circuit. Clearly these claims are directed to statutory subject matter.

Thus, for at least these reasons, Applicants respectfully request that the rejections under § 101 be withdrawn.

Rejection Under 35 U.S.C. §112, First Paragraph

The Office Action rejects claims 1 and 3 - 24 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. As set forth above, Applicants have canceled claims 13, 20, 21, 23 and 24, and respectfully assert that the rejection as to these claims has been rendered moot. With respect to the remaining claims, Applicants respectfully traverse.

In this regard, Applicants have amended claims 1, 3 – 6, 10, 14 – 17, 19 and 22 and respectfully assert that the rejections have been accommodated. However, to the extent that the rejections are otherwise improper for lacking in legal basis, Applicants respectfully assert that claims the pending claims are in compliance with the written description requirement.

Specifically, the Office Action appears to indicate that the disclosure does not teach the various registers and associated functionality recited in the claims. Applicants respectfully disagree.

With respect to the "first register" (such as recited in claim 1), the disclosure teaches that the register BuffSects 505 contains a value corresponding to the number of sectors in the buffer 205 (*see* Table 1, for example). With respect to the "second register" (such as recited in claim 1), the disclosure teaches that the register BuffSects 505 is decremented by the value contained in the register SPB 504 (*see* page 8, line 25 to page 9, line 2; "the values of HXSC 502 and BuffSects 505 are decreased by the value of SPB 504. . .").

With respect to the limitations in claim 4, for example, the disclosure teaches that the register Host_LWPtr 511 stores an address representing a location in the buffer where data is being transferred between the buffer and the host device. Additionally, the disclosure teaches that the register SMI_LW_Ptr 512 stores an address representing a location in the buffer where data is being transferred between the buffer and the storage medium.

With respect to the limitations in claim 5, for example, the disclosure teaches that the register SOB_LW_Ptr 515 an address representing a beginning of the buffer. Additionally, the disclosure teaches that the register EOB_LW_Ptr 516 stores an address representing an end of the buffer.

With respect to the limitations in claim 6, for example, the disclosure teaches that the register MaxBuffSects 510 stores a value representing a storage capacity of the buffer.

Thus, Applicants respectfully assert that the rejections are improper in that the disclosure fully supports the limitations recited in each of claims 1, 3 – 12, 14 – 19, 22, 25 and 26. Additionally, with respect the portion of the rejection indicating that there is no functional relationship between the elements in the claims, Applicants respectfully assert that this portion of the rejection is similarly improper. That is, all of the recited elements are involved with the transfer of data between a host device and a storage medium, many of which expressly recite a direct functional relationship to the buffer. Therefore, for at least these reasons, Applicants respectfully assert that the rejection is improper and requests that the rejections under 35 U.S.C. § 112, first paragraph be removed.

Rejection Under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 1 - 8 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. As set forth above, claim 2 was previously canceled. With respect to the remaining claims, Applicants respectfully traverse.

In this regard, Applicants have amended claims 1 and 3 – 6, and respectfully assert that the rejections have been accommodated. However, to the extent that the rejections are otherwise improper for lacking in legal basis, Applicants respectfully assert that claims 1 and 3 – 8 are in compliance with the provisions of 35 U.S.C. § 112, second paragraph.

Specifically, the Office Action appears to indicate that the disclosure does not teach the various registers and associated functionality recited in the claims. Applicants respectfully disagree.

With respect to the "first register" (such as recited in claim 1), the disclosure teaches that the register BuffSects 505 contains a value corresponding to the number of sectors in the buffer 205 (*see* Table 1, for example). With respect to the "second register" (such as recited in claim 1), the disclosure teaches that the register BuffSects 505 is decremented by the value contained in the register SPB 504 (*see* page 8, line 25 to page 9, line 2; "the values of HXSC 502 and BuffSects 505 are decreased by the value of SPB 504. . .").

With respect to the limitations in claim 4, for example, the disclosure teaches that the register Host_LWPtr 511 stores an address representing a location in the buffer where data is being transferred between the buffer and the host device. Additionally, the disclosure teaches that the register SMI_LW_Ptr 512 stores an address representing a location in the buffer where data is being transferred between the buffer and the storage medium.

With respect to the limitations in claim 5, for example, the disclosure teaches that the register SOB_LW_Ptr 515 an address representing a beginning of the buffer. Additionally, the disclosure teaches that the register EOB_LW_Ptr 516 stores an address representing an end of the buffer.

With respect to the limitations in claim 6, for example, the disclosure teaches that the register MaxBuffSects 510 stores a value representing a storage capacity of the buffer.

Thus, Applicants respectfully assert that the rejections are improper and should be removed. Additionally, with respect the portion of the rejection indicating that there is no functional relationship between the elements in the claims, Applicants respectfully assert that this portion of the rejection is similarly improper. That is, all of the recited elements are involved with the transfer of data between a host device and a storage medium, many of which expressly recite a direct functional relationship to the buffer. Therefore, for at least these reasons, Applicants respectfully assert that the rejection is improper and requests that the rejections under 35 U.S.C. § 112, first paragraph be removed.

Rejections Under 35 U.S.C. §102

The Office Action indicates that claims 1 and 7 - 9 stand rejected under 35 U.S.C. 102(b) as being anticipated by *Siegel*. Applicants respectfully traverse the rejection.

With respect to *Siegel*, *Siegel* teaches the use of a base count register that keeps track of the number of bytes that are left to be transferred. However, in order to determine whether transferred data is present in a buffer during a transfer, a decision is made whether the cache RAM buffer address corresponding to the address of the DMA controller 36 currently contains transferred data. Thus, *Siegel* analyzes address usage to monitor data transfer to the buffer. This is in direct contrast to the limitations recited in Applicants' claims that generally involve the use of registers to track such transfers. Moreover, Applicants respectfully assert that it is improper to attribute any teaching of a buffer to Applicants' claimed register, as Applicants have clearly and distinctly recited a buffer in addition to a register.

Notably, *Sefidvash* does not remedy the aforementioned deficiencies of *Siegel*. In this regard, the Office Action appears to summarily conclude that, because *Sefidvash* teaches the

use of registers "wherein each of the registers perform their own tasks (see Office Action at page 12). However, the tasks performed by the registers of *Sefidvash* are not associated with the limitations recited in Applicants' claims.

In this regard, Applicants have amended claim 1 to recite:

> 1. A method for transferring data between a host device and a storage medium via a buffer, comprising:
> receiving from the host device a command to transfer data between the host device and the storage medium;
> storing in a first register a value for tracking a number of data units that have been transferred into the buffer but that have not yet been transferred out of the buffer;
> ***storing in a second register a value corresponding to a number of data units to be transferred during an iteration of the transfer of the data between the host device and the storage medium***;
> transferring at least some of the data into the buffer responsive to the command;
> ***modifying the value contained in the first register with the value stored in the second register in response to a completed iteration of the transfer of the data into the buffer***;
> transferring at least some of the data out of the buffer; and
> modifying the value contained in the first register in response to a transfer of a data unit out of the buffer;
> ***wherein, during the transfer of the data between the host device and the storage medium, the value contained in the first register corresponds to a number of data units currently stored in the buffer.***

(Emphasis Added).

Applicants respectfully assert that *Siegel* is legally deficient for the purpose of anticipating claim 1. Specifically, Applicants respectfully assert that *Siegel* does not teach or otherwise disclose at least the features/limitation emphasized above in claim 1. In this regard, *Siegel* analyzes address usage to monitor data transfer to the buffer and is not involved with "modifying the value contained in the first register with the value stored in the second register in response to a completed iteration of the transfer of the data into the buffer," as recited in claim 1. Notably, Applicants have amended claim 1 to incorporate the term "iteration," which Applicants have used in accordance with its common and ordinary meaning. No new matter has been added as is clearly indicated by the iterative data transfer process depicted in

FIG. 3, for example, and the accompanying description. Therefore, Applicants respectfully assert that the rejection is improper and requests that the claim 1 be placed in condition for allowance.

Since claims 7 - 9 are dependent claims that incorporate the limitations of claim 1, Applicants respectfully request that the rejection of the claims under 35 U.S.C. 102(b) also be removed.

Rejections Under 35 U.S.C. §103

The Office Action indicates that claims 3 – 6 and 10 - 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Siegel* and *Sefidvash*. As set forth above, Applicants have canceled claims 13, 20, 21, 23 and 24, and respectfully assert that the rejection as to these claims has been rendered moot. With respect to the remaining claims, Applicants respectfully traverse.

In this regard, Applicants have amended claims 1, 3 – 6, 10, 14 – 17, 19 and 22 and respectfully assert that the rejections have been accommodated. In particular, Applicants have amended claim 1 to recite:

> 1. A method for transferring data between a host device and a storage medium via a buffer, comprising:
> receiving from the host device a command to transfer data between the host device and the storage medium;
> storing in a first register a value for tracking a number of data units that have been transferred into the buffer but that have not yet been transferred out of the buffer;
> ***storing in a second register a value corresponding to a number of data units to be transferred during an iteration of the transfer of the data between the host device and the storage medium***;
> transferring at least some of the data into the buffer responsive to the command;
> ***modifying the value contained in the first register with the value stored in the second register in response to a completed iteration of the transfer of the data into the buffer***;
> transferring at least some of the data out of the buffer; and

modifying the value contained in the first register in response to a transfer of a data unit out of the buffer;

wherein, during the transfer of the data between the host device and the storage medium, the value contained in the first register corresponds to a number of data units currently stored in the buffer.

(Emphasis Added).

Applicants respectfully assert that the cited art, either individually or together, is legally deficient for the purpose of rendering claim 1 unpatentable. Specifically, Applicants respectfully assert that neither *Siegel* nor *Sefidvash* teaches or reasonably suggests at least the features/limitation emphasized above in claim 1. In this regard, *Siegel* analyzes address usage to monitor data transfer to the buffer and is not involved with "modifying the value contained in the first register with the value stored in the second register in response to a completed iteration of the transfer of the data into the buffer," as recited in claim 1. Moreover, *Sefidvash* teaches the use of registers, but not in the particular manner recited in claim 1. Therefore, Applicants respectfully assert that claim 1 is in condition for allowance.

Since claims 3 – 9, 25 and 26 are dependent claims that incorporate all the features/limitations of claim 1, Applicants respectfully assert that these claims also are in condition for allowance. Additionally, these claim recites other features/limitations that can serve as an independent basis for patentability.

With respect to claim 10, that claim has been amended to recite:

10. A data transfer system for transferring data between a host device and a storage medium, comprising:

a host interface operative to receive from the host device a command to transfer data between the host device and the storage medium;

a buffer operative to temporarily store data that is transferred between the host device and the storage medium;

a first register operative to store a value for tracking a number of data units that have been transferred into the buffer but that have not yet been transferred out of the buffer; and

a second register operative to store a value for modifying the value contained in the first register, the value stored in the second register corresponding to a number of data units to be transferred during an iteration of the transfer of the data between the host device and the storage medium;

wherein, in transferring the data between the host device and the storage medium, the value contained in the first register corresponds to a number of data units currently stored in the buffer.

(Emphasis Added).

Applicants respectfully assert that the cited art, either individually or together, is legally deficient for the purpose of rendering claim 10 unpatentable. Specifically, Applicants respectfully assert that neither *Siegel* nor *Sefidvash* teaches or reasonably suggests at least the features/limitation emphasized above in claim 10. In this regard, *Siegel* analyzes address usage to monitor data transfer to the buffer and is not involved with "a second register operative to store a value for modifying the value contained in the first register, the value stored in the second register corresponding to a number of data units to be transferred during an iteration of the transfer of the data between the host device and the storage medium," as recited in claim 10. Moreover, *Sefidvash* teaches the use of registers, but not in the particular manner recited in claim 10. Therefore, Applicants respectfully assert that claim 10 is in condition for allowance.

Since claims 11, 12 and 14 - 18 are dependent claims that incorporate all the features/limitations of claim 10, Applicants respectfully assert that these claims also are in condition for allowance. Additionally, these claim recites other features/limitations that can serve as an independent basis for patentability.

With respect to claim 19, that claim has been amended to recite:

19. A method for transferring data between a host device and a storage medium via a buffer, comprising:

receiving from the host device a command to transfer data between the host device and the storage medium;

storing in a first register a value indicative of an amount of data that can be currently stored in the buffer;

incrementing the value contained in the first register by a value contained in a second register in response to an iteration of a data transfer into the buffer, the value in the second register corresponding to a number of data units to be transferred during the iteration of the transfer of the data between the host device and the storage medium; and

decrementing the value contained in the first register in response to a data transfer out of the buffer.

(Emphasis Added).

Applicants respectfully assert that the cited art, either individually or together, is legally deficient for the purpose of rendering claim 19 unpatentable. Specifically, Applicants respectfully assert that neither *Siegel* nor *Sefidvash* teaches or reasonably suggests at least the features/limitation emphasized above in claim 19. In this regard, *Siegel* analyzes address usage to monitor data transfer to the buffer and is not involved with "incrementing the value contained in the first register by a value contained in a second register in response to an iteration of a data transfer into the buffer," as recited in claim 19. Moreover, *Sefidvash* teaches the use of registers, but not in the particular manner recited in claim 19. Therefore, Applicants respectfully assert that claim 19 is in condition for allowance.

With respect to claim 22, that claim has been amended to recite:

> 22. An application specific integrated circuit (ASIC) for transferring data between a host device and a storage medium, comprising:
>
> a buffer that temporarily stores data that is transferred between the host device and the storage medium;
>
> ***a first register that stores a value corresponding to an amount of data that can be currently stored in the buffer***; and
>
> ***a second register that stores a value corresponding to a number of data units to be transferred to the buffer such that, responsive to the number of data units being transferred into the buffer, the value stored in the first register is incremented with the value contained in the second register***;
>
> ***wherein, in response to a data transfer out of the buffer, the value contained in the first register is decremented by a value corresponding to a number of data units transferred out of the buffer.***

(Emphasis Added).

Applicants respectfully assert that the cited art, either individually or together, is legally deficient for the purpose of rendering claim 22 unpatentable. Specifically, Applicants respectfully assert that neither *Siegel* nor *Sefidvash* teaches or reasonably suggests at least the features/limitation emphasized above in claim 22. In this regard, *Siegel* analyzes address usage to monitor data transfer to the buffer and is not involved with "a second register that

stores a value corresponding to a number of data units to be transferred to the buffer such that, responsive to the number of data units being transferred into the buffer, the value stored in the first register is incremented with the value contained in the second register;

wherein, in response to a data transfer out of the buffer, the value contained in the first register is decremented by a value corresponding to a number of data units transferred out of the buffer," as recited in claim 22. Moreover, *Sefidvash* teaches the use of registers, but not in the particular manner recited in claim 22. Therefore, Applicants respectfully assert that claim 22 is in condition for allowance.

Newly Added Claims

In this response Applicant has added new claims 25 and 26. No new matter has been added. In this regard, Applicant respectfully asserts that these claims are in condition for allowance for at least the reason that these claims are dependent claims that incorporate the limitations of claim 1, the allowability of each of which is set forth above. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability.

Cited Art Made of Record

The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

M. Paul Qualey, Jr.; Reg. No. 43,024

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
Suite 1750
100 Galleria Parkway N.W.
Atlanta, Georgia 30339
(770) 933-9500

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 5/30/06.

Stephanie Riley
Signature